REMARKS

Claims 1-11 are all the claims pending in the application. Claims 5-9 and 11 are allowed.

Claims 1-4 and 10 are rejected under 35 U.S.C. § 102(e) as being anticipated by Wu et al. (US 6,108,046). Claim 1 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Hatano et al. (US 5,933,196). Claims 2-4 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Hatano et al. in view of Wu et al. Applicant respectfully traverses the rejections as set forth below.

The present invention relates to an apparatus and method for selectively converting a clock frequency in a digital signal receiver. A non-limiting, exemplary embodiment of the present invention shown in FIG. 3, includes a first phase locked loop 208a, a second phase locked loop 208b, a switching portion 208c for selecting a clock frequency from one of the first and second phase locked loops according to a predetermined control signal; and a controller 212 for controlling the switching portion to select and output the clock frequency corresponding to a frame rate of an input digital signal.

Wu et al. relates to a method and apparatus for automatically detecting the format of a television signal at a video encoder to allow proper encoding of the signal, especially for detecting high-definition television (HDTV) formats. FIG. 2 illustrates a detailed view of a video format detector circuit according to Wu et al. In FIG. 2, the divider 220, PD 216, active filter 224, VCXO 226, and the path between the VCXO 226 and the divider 220 form a phase-locked loop (PLL). Also, the dividers 238 and 230, PD 218, active filter 234, VCXO 236, and the path between the VCXO 236 and the divider 238 form a PLL.

Hatano et al. relates to a pixel conversion apparatus. Shown in FIG. 6 is a pixel conversion apparatus in accordance with a first exemplary embodiment of Hatano et al. In FIG. 6, the block 61 is a sync separator. The block 62 is a first PLL circuit for generating a first clock signal synchronizing with a horizontal sync signal of the input signal. The block 63 is a second PLL circuit for generating a second clock signal synchronizing with a horizontal sync signal of the input signal. The block 64 is a scanning line converter for converting the number of scanning lines of the input signal. The block 65 is a timing signal generator for generating an interpolation coefficient and an interpolation timing signal to interpolate the sample at scanning line converter 64 and generating a sync signal to drive a display device such as a liquid crystal panel.

Rejection of claims 1-4 and 10 based on Wu et al.

Applicant submits that Wu et al. fail to teach or suggest the format converter feature of claim 1 of the present invention. Wu et al. perform format detection (col. 2, lines 48-55), but do not teach or suggest a format converter for receiving either of a first input digital signal and a second input digital signal, according to which of the first and second input digital signals is present, the format converter for converting the input digital signal received by the format converter into a predetermined display format output signal. Instead, Wu et al. simply disclose a single input video signal (col. 4, lines 4-12), the format of which is determined (col. 4, lines 39-41).

Furthermore, it appears on page 9 of the Office Action that the Examiner may have relied, at least in part, on this feature to find claims 5-9 and 11 to be allowable.

Therefore, Applicant submits that claim 1 and its dependent claims 2-4 are allowable.

Similarly, Wu et al. do not teach or suggest outputting the selected clock frequency to components of the digital signal receiver that use the clock frequency to convert the input broadcast signal into a predetermined display format output signal, as required by claim 10. Hence, claim 10 is allowable as well.

Also, Applicant amends claim 11 to correct its dependency, thereby making claim 11 depend from claim 10.

Rejection of claim 1 based on Hatano et al.

Applicant submits that Hatano et al. also fail to teach or suggest the claimed format converter of claim 1. Instead of disclosing the above-noted limitation of claim 1, Hatano et al. disclose only a single input signal, which undergoes pixel conversion. See, for example, abstract; col. 6, line 66 – col. 7, line 12. Hence, Hatano et al. do not disclose all of the limitations of amended claim 1.

Furthermore, even if the Examiner's assertion that Hatano et al. disclose some sort of control mechanism or switch or controller is correct, the reference still fails to teach or suggest the specifically claimed limitations of claim 1. The Examiner cannot simply assume that explicit limitations of a claim or claims are disclosed by a reference, merely because the reference may disclose a related element. Thus, Applicant respectfully submits that the rejection of claim 1 based on Hatano et al. is improper.

Therefore, claim 1 is allowable over Hatano et al. for at least these reasons.

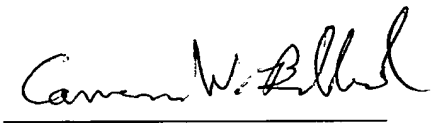
Rejection of claims 2-4 and 10 based on Hatano et al. in view of Wu et al.

Since Hatano et al. and Wu et al. fail to teach or suggest all of the limitations of the claims, as discussed above, Applicant submits that claims 2-4 and 10 are allowable over the combination of Hatano et al. and Wu et al.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

The claims are amended as follows:

1. (Amended) An apparatus for selectively converting a clock frequency in a digital signal receiver, comprising:

a first phase locked loop;

a second phase locked loop;

a switching portion for selecting a clock frequency from one of the first and second phase locked loops according to a predetermined control signal; [and]

a format converter for receiving either of a first input digital signal and a second input digital signal, according to which of the first and second input digital signals is present, the format converter for converting the input digital signal received by the format converter into a predetermined display format output signal; and

a controller for controlling the switching portion to select and output the clock frequency corresponding to a frame rate of [an] the input digital signal.

10. (Amended) A method of adapting clock frequency [frequencies] in digital signal receiver to correspond with a frame rate of an input broadcast signal, said method comprising:

receiving said input broadcast signal into said digital signal receiver;

detecting a frame rate of the input broadcast signal received;

selecting a clock frequency that corresponds to the frame rate which is detected; and

outputting the clock frequency which is selected to components of the digital signal receiver that use the clock frequency to convert the input broadcast signal into a predetermined display format output signal [decode and display said input broadcast signal].

11. (Amended) The method according to claim [7] 10 wherein the step of selecting the clock frequency comprises, outputting a control signal from a controller, said control signal depending upon the frame rate which is detected; receiving said control signal into a selector, said selector connected to outputs of a plurality of phase locked loops, wherein each phase locked loop has a predetermined clock frequency, and selecting one predetermined clock frequency of one of said plurality of phase locked loops based upon the control signal received by the selector.